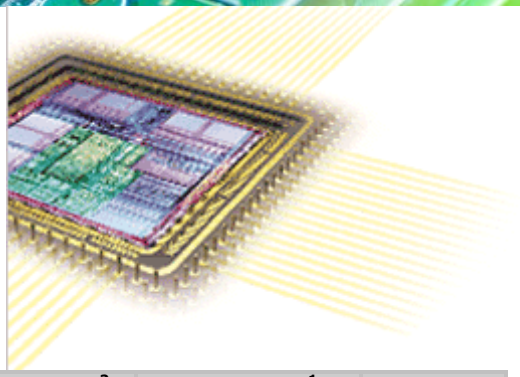
ntAWGN-HT

High Throughput Gaussian Channel Emulator



The performance evaluation of a telecom system under the presence of noise using software can be very time consuming. Whereas the noise generation in the analog domain is an easy task, in digital domain the generation of AWGN is a much more complex task. The ntAWGN-HT core provides a hardware implementation of an accurate AWGN noise generator that can be used in the efficient performance evaluation of a digital communication system. The ntAWGN-HT core implements a high speed AWGN channel emulator ideal for measuring the bit error rate (BER) performance of a communication system supporting a throughput rate up to 12.8 Gbps.

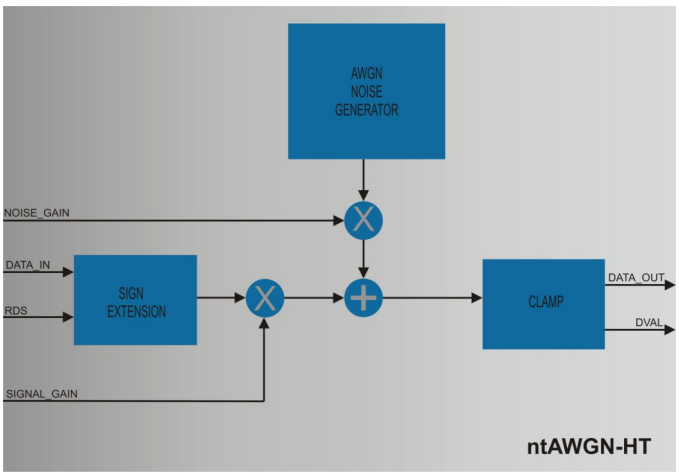
Silicon Vendor	Device[2]	Resources [1]	Fmax (MHz)
Xilinx	Virtex5	5080 CLB Slices / 192 DSP48E / 32 Block RAMs	200

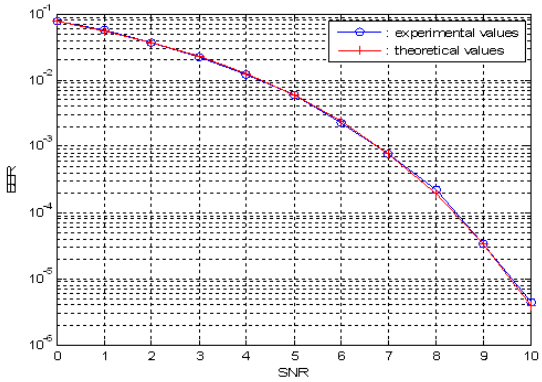
1)Effective throughput rate is 12.8 Gbps. 2)Speed grade1.

Applications

- Any telecom application that requires accurate emulation of an AWGN channel.
- Bit-error rate measurement systems.

Block Diagram





Theoretical vs AWGN-HT BER vs SNR for uncoded BPSK

Features

- High speed AWGN Channel emulator based on the Box-Muller algorithm and the Central Limit Theorem.

FLEXIBILITY

- High periodicity of the generated noise samples. Period is ~ 2100 .
- Probability density function (pdf) deviates less than 1 % from the Gaus sian pdf for |x| up to 4σ.
- Generics allow modification of arithmetic precision, number of accumulations, lfsr's initialization.
- Noise gain input is 8 bit wide with 2 bits of integer and 6 bits of fraction. Dynamic range is from 0.0 to 4.0. Step is 2-6.
- Noise is 16 bit wide with 6 bits of integer and 10 bits of fractional part.

HIGH PERFORMANCE

- Design optimized for Xilinx Virtex5 FPGA technology.
- Maximum clock rate of 200MHz (Virtex-5, speed grade -1).
- Compact design that requires approximately 5000 Virtex-5 CLB slices and 192 DSP48Es.

OTHERS

- Fully synchronous design, using single clock.
- Silicon proven in Xilinx FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntAWGN_HT core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Matlab model.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntAWGN_HT core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request.

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