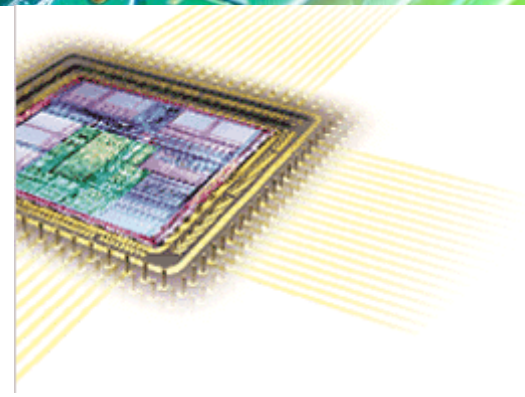


# ntG711\_CMP

## G711 Compressor



The ntG711\_CMP core implements the ITU G.711 compliant compressing. The G.711 standard specifies a compressing function for 16-bit uniform PCM to 8-bit A/ $\mu$ -law word. The ntG711\_CMP core is programmable and its functionality is controlled by the following control bits.

**law** : This bit selects the coding rule to be used. When '0'  $\mu$ -law is selected, when '1' A-law is selected.

**A\_inv\_dis** : This bit activates/disactivates the inversion of even bits of the output word for the A-law case.

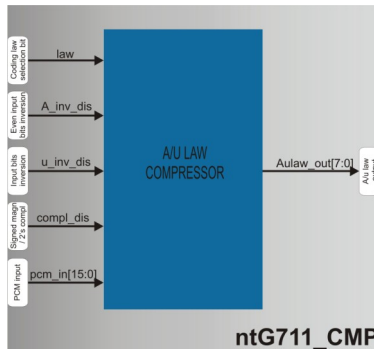
**u\_inv\_dis** : This bit activates/disactivates the inversion of bits of the output word for the  $\mu$ -law case.

**comp\_dis** : This bit selects the representation format of the output vector. When '0' is in 2's complement format, when '1' is in sign magnitude format.

### Applications

The ntG711\_CMP core can be used in a variety of applications, including PCM codecs, voice companding and front-end for any DSP processing of 64 kbps voice.

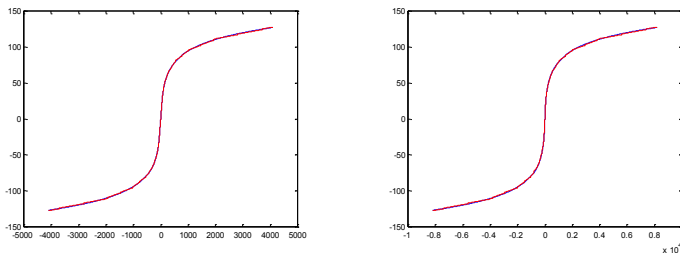
### Block Diagram



### Features

- Compresses 16 bit linear PCM to 8 bit  $\alpha$ -law or  $\mu$ -law logarithmic PCM.
- Compliant to the ITU-G.711 standard.
- Purely combinational logic RTL implementation.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

### Performance



The ntG711\_CMP PCM to A-law transformation and PCM to  $\mu$ -law transformation.

The figures above illustrate the comparison of the ntG711\_CMP a-law and  $\mu$ -law compressing function (red line) with the equivalent matlab theoretical model (blue line).

### Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon	Device	Resources
Xilinx	Virtex 5	54 CLB Slices
TSMC	0.18 um	610 gates <sup>1</sup>

1. Equivalent NAND2 gate count.

### Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntG711\_CMP core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Matlab code.
- Comprehensive technical documentation.
- Technical support.

### Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

### Ordering information

To purchase or make any further inquiries about our ntG711\_CMP core, or any other Noesis Technologies products or services, contact us at [info@noesis-tech.com](mailto:info@noesis-tech.com). Noesis Technologies products are purchased under a License Agreement, copies of which are available on request.