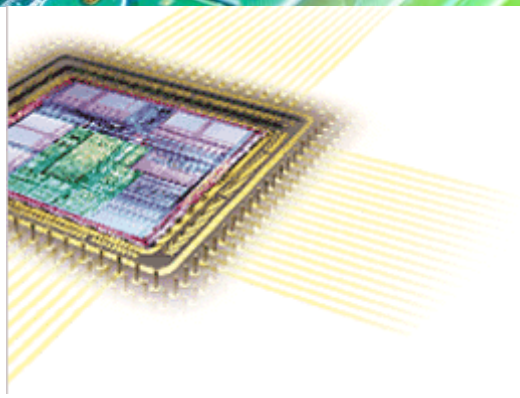
ntCVSD

Continuously variable slope delta modulation



The growth in wireless communication systems, cellular mobile radio and VoIP technology has created the imperative need for bandwidth efficient, high speed quality voice coding algorithms. The fundamental principle of the CVSD algorithm is the encoding of one bit per sample. For example an audio signal sampled at 32 KHz will be compressed to 32 Kbps.

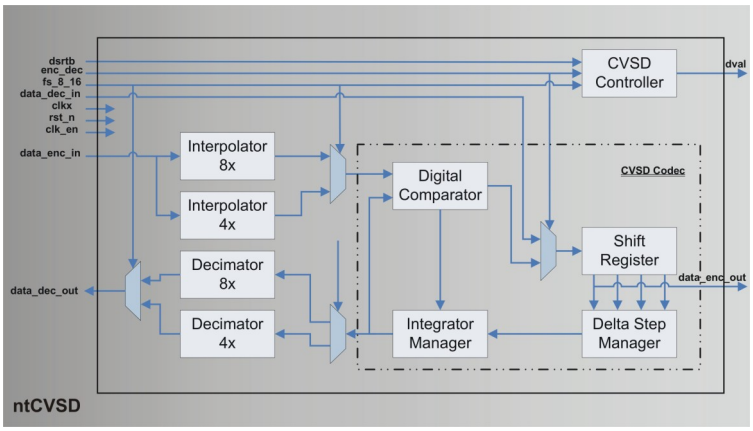
The ntCVSD codec IP core can be configured to operate either as an encoder or as a decoder functional block. In encoder mode the core accepts input data at a rate of 8 KHz/128 Kbps or 16KHz/256Kbps and are sampled when the data strobe signal is asserted high. Higher input sampling data rates can also be supported with no up-sampling provision. The sampled input data can either be initially up-sampled to 64 KHz by using an interpolation filter in order to improve speech/audio quality before entering into the actual CVSD codec unit or can be just directly fed into the CVSD codec unit with no previous processing. These samples are then driven to a digital comparator in order to be compared with a reference signal value. If the input sample is greater than the reference signal then a logic 1 is transmitted and a step value is added on the reference signal. If the input sample is less than the reference signal then a logic 0 is transmitted and a step value is subtracted from the reference signal. The transmitted bits are also stored in an N-bit shift register. Depending on the shift register contents, a decision is made whether a slope overload has occurred and the step value is adjusted accordingly in order to keep up with the changing slope of the input waveform. Depending on both the digital comparator and the slope overload decisions, an integrator estimation is generated in order to approximate the previous input value and drive it back to the digital comparator.

In decoder mode the core accepts the compressed bit-stream and the incoming bits are sampled when the data strobe signal is asserted high. The received bit-stream is fed directly to the N-bit shift register and depending on the shift register contents, a decision is made whether a slope overload has occurred. The uncompressed signal is reconstructed through the integrator unit. The reconstructed output will be either be fed into the decimation filter to be down-sampled at the original sampling rate and then driven at the output or will be just directly driven at the output with no previous processing.

Applications

The ntCVSD codec is designed to compress 16-bit PCM speech/audio data for transmission in telecom networks or to decompress a received CVSD encoded bitstream. It is compatible with legacy CVSD implementations and fully compliant with the Bluetooth CVSD specification.

Block Diagram



Features

- CVSD compression and decompression algorithm.
- The core can be configured either as a CVSD encoder or as a CVSD decoder.
- Support for 16-bit PCM speech input (sampled at 8 KHz) or audio input (sampled at 16 KHz).
- Higher sampling rates can also be supported.
- Innovative fully digital CVSD algorithm implementation, no requirement for analog parts.
- Verified speech quality with ITU-T PESQ model.
- Compliant with legacy CVSD implementations.
- Compliant with Bluetooth CVSD specification.
- Portable to any FPGA/ASIC technology.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources [1]	Fmax (MHz)
Xilinx	Virtex 6	349 CLB Slices / 31 DSP Slices	95

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntCVSD core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA or ASIC technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Matlab model.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntCVSD core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

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