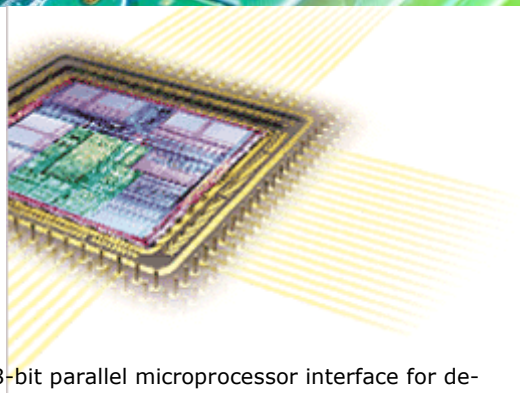
ntE1_G704

G704-E1 Framer/Deframer

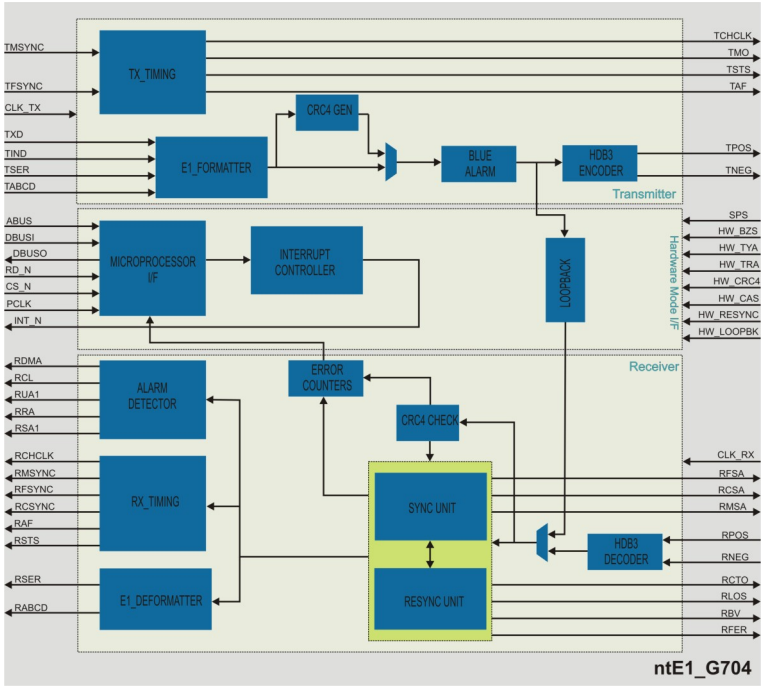


Noesis Technologies ntE1_G704 Framer/Deframer is designed for E1 networks and is compliant with ITU recommendations G.704, G.706, G.732, G.775 and O.163. The core provides all the necessary data formatting transforms for transmission over an E1 carrier. E1 is one of the two most widely used TDM (time division multiplexing) carriers incorporating 32 channels, each with a bandwidth of 64 kbps providing a total bit rate of 2048 kbps. The ntE1_G704 IP core provides a flexible interface supporting hardware and microprocessor modes. Specifically the core can be connected to a host system either through an 8-bit parallel microprocessor interface (HP mode) or through a set of I/O ports (HW mode). When in HP mode, the microprocessor configures and monitors the functionality of the core through a rich set of registers. When in HW mode, the core is directly controlled and monitored through a set of dedicated ports and no microprocessor control is necessary. At the transmit side, the framer generates framing patterns, CRC4 bits, formats outgoing and signalling data, generates alarms and clock outputs for data conditioning and decoding. At the receive side, the deframer establishes frame / multiframe synchronization, extracts data, signalling and alarm flags. It provides information like frame, multiframe alignment, calculates CRC4, counts CRC4 errors and performs A-bit processing.

Applications

The ntE1_G704 core can be used in primary rate digital trunk interfaces, computer to PBX interfaces (CPI and DMI), to any high speed computer-to-computer data link and generally, to any digital cross connect interface.

Block Diagram



Features

- E1 framer/deframer compliant to G.704, G.706, G.732, G.775 and O.163 CCITT recommendations.
- Supports CAS and CCS signaling standards.
- Supports CRC4 based framing standards.
- User configurable receive and transmit control.
- Supports 8-bit parallel microprocessor interface for device configuration and control in host processor mode.
- Hardware control mode requires no host processor; ideal for stand-alone applications.
- Supports HDB3 line coding.
- Supports loop-back mode.
- Alarm generation, alarm detection and error logging.
- Compatible with Dallas DS2186 transmit line interface.
- Fully synchronous design.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources [1]	Fmax (MHz)
Xilinx	Spartan 3	1027 CLB Slices	102 (clk_tx) 107 (clk_rx) 207 (pclk)
Altera	Stratix-III	887 ALUTs	230 (clk_tx) 244 (clk_rx) 480 (pclk)
TSMC	0.18 um	9200 gates [2]	400 (clk_tx) 432 (clk_rx) 770 (pclk)

1. The implementation is speed optimized. Please contact us for area optimized results. 2. Equivalent NAND2 gate count.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntE1_G704 core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntE1_G704 core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

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