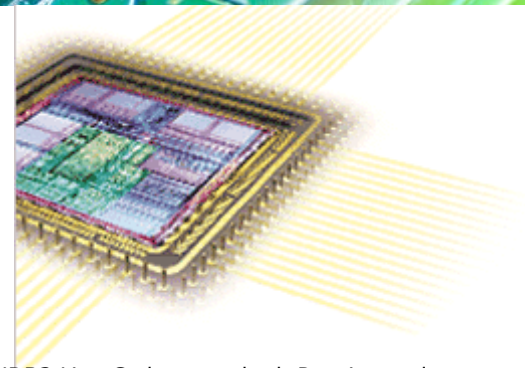


# ntE2\_E3 G742/G751 E2/E3 Framer/Deframer

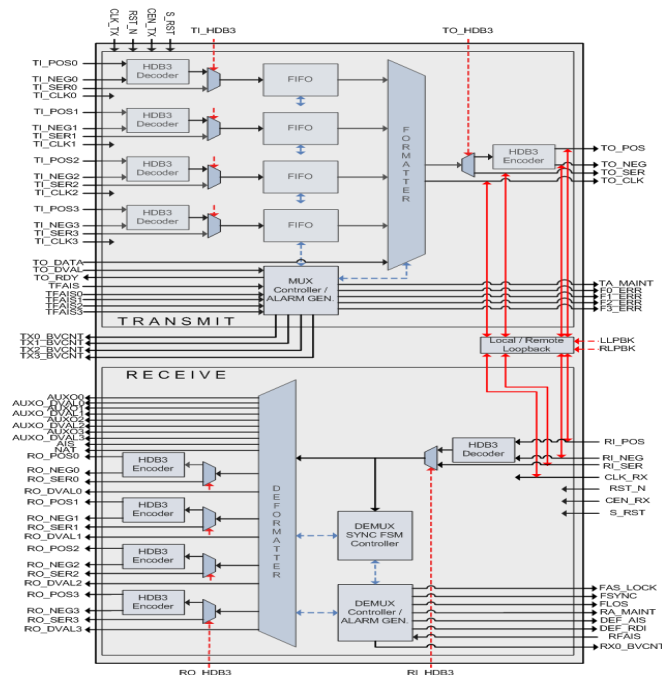


Noesis Technologies ntE2\_E3 Framer/Deframer is designed for E2/E3 networks and supports all requirements of ITU recommendations G.742, G.751 and G.775. The core provides all the necessary data formatting transforms for transmission over E2/E3 networks. The device can be controlled through a simple set of dedicated ports, allowing robust operation. One ntE2\_E3 core instance can operate either as an E1/E2 (2.048/8.448 Mbps) rate Multiplexer/Demultiplexer, or as an E2/E3 (8.448/34.368 Mbps) rate Multiplexer/Demultiplexer. In addition five ntE2\_E3 cores can be instantiated to operate as an E1/E3 (2.048/34.368 Mbps) rate Multiplexer/Demultiplexer. The transmit side of the framer generates framing patterns, transmits the alarm and the national bits, interleaves the four tributaries into the high level data stream, calculates the justification mechanism status and the nature of the stuffing bits available, as well as generates alarms, status bits, and clock outputs. The receive side establishes frame synchronization, extracts the interleaved data, the alarm and national bits as well as the auxiliary channels data, monitors for error conditions and generates alarm flags, data valid bits, status bits and clock outputs. The HDB3 codecs can be either used or bypassed, on both transmit and receive sides, depending on the application. Finally both local and remote loopback features are available.

## Applications

The ntE2\_E3 core can be used in secondary or tertiary rate digital trunk interfaces, computer to PBX interfaces (CPI and DMI), to any high speed computer-to-computer data link and generally, to any digital cross connect interface.

## Block Diagram



## Features

- E2/E3 framer/deframer compliant to G.742, G.751, G.775 ITU-T standards.
- Performs four E1 to one E2 or four E2 to one E3 multiplexing and vice-versa demultiplexing.
- Five ntE2\_E3 cascaded cores implement a sixteen E1 to one E3 Multiplexer/Demultiplexer.

- Optional HDB3 Line Codecs one both Receive and Transmit sides.
- Local and Remote Loop-back modes.
- Configurable Frame Alignment Signal.
- User access to the Alarm bit and the National bit.
- User access to four low speed Auxiliary Channels, one per multiplexed tributary, available via unused Stuffing bits.
- Fully synchronous and parametric design.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

## Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources	Fmax (MHz)
Xilinx	Virtex 6	436 Slices <sup>1</sup>	170 (clk_tx) 250 (clk_rx)
Xilinx	Virtex 6	406 Slices <sup>2</sup>	186 (clk_tx) 205 (clk_rx)

1. E2 mode (2 Mbps / 8 Mbps) 2. E3 mode (8 Mbps / 34 Mbps)

## Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntE2\_E3 core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Comprehensive technical documentation.
- Technical support.

## Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

## Ordering information

To purchase or make any further inquiries about our ntE2\_E3 core, or any other Noesis Technologies products or services, contact us at [info@noesis-tech.com](mailto:info@noesis-tech.com). Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .