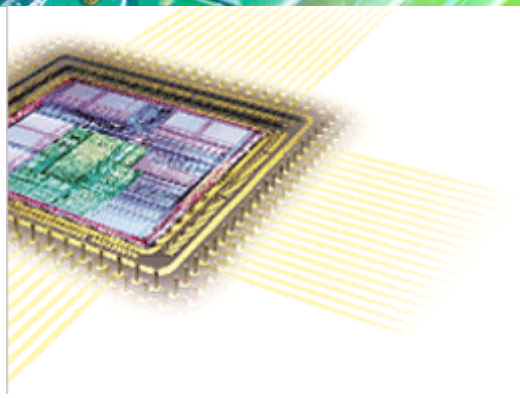
ntG711_EXP

G711 Expander



The ntG711_EXP core implements the ITU G.711 compliant expanding. The G.711 standard specifies a translation for 8-bit A/μ-law in 14 -bit uniform PCM word. The ntG711_EXP core is programmable and its functionality is controlled by the following control bits.

law : This bit selects the coding rule to be used. When '0' μ-law is selected, when '1' A-law is selected.

A_inv_dis : This bit activates/disactivates the inversion of even bits of the input word for the A-law case.

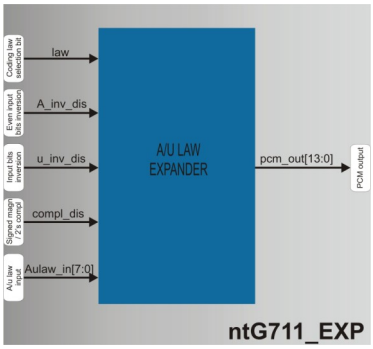
u_inv_dis : This bit activates/disactivates the inversion of bits of the input word for the μ-law case.

comp_dis : This bit selects the representation format of the output vector. When '0' is in 2's complement format, when '1' is in sign magnitude format.

Applications

The ntG711_EXP core can be used in a variety of applications, including PCM codecs, voice companding and front–end for any DSP processing of 64 kbps voice.

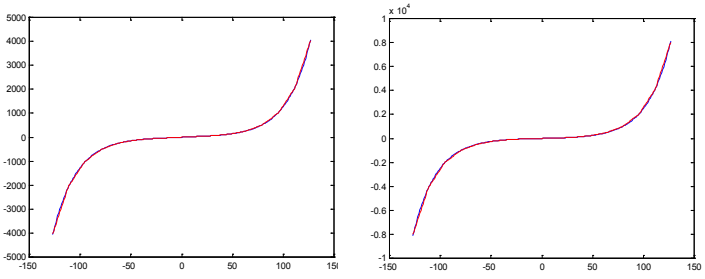
Block Diagram



Features

- Expands 8 bit a-law or μ-law logarithmic PCM to 13/14 bit linear PCM.
- Compliant to the ITU-G.711 standard.
- Purely combinational logic RTL implementation.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Performance



The ntG711_EXP A-law to PCM transformation and μ-law to PCM transformation.

The figures above illustrate the comparison of the ntG711_EXP a-law and μ-law expanding function (red line) with the equivalent matlab theoretical model (blue line).

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon	Device	Resources
Xilinx	Virtex 5	75 CLB Slices / 1 DSP48E
TSMC	0.18 um	720 gates [1]

1. Equivalent NAND2 gate count.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntG711_EXP core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Matlab code.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntG711_EXP core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

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