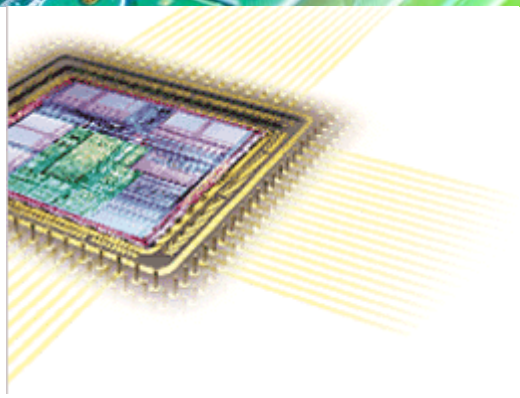
ntLDPCD

Fully Configurable LDPC Decoder



In channel coding redundancy is inserted in the transmitted information bit-stream. This redundant information is used in the decoder to eliminate the channel noise. The error correction capability of a FEC system strongly depends on the amount of redundancy as well as on the coding algorithm itself. The Low Density Parity Check (LDPC) codes are powerful capacity-approaching channel codes and have exceptional error-correction capabilities. In addition, LDPC codes are suited for implementations that make heavy use of parallelism. The ntLDPCD IP core utilizes the Quasi-Cyclic LDPC Block Codes (QC-LDPC-BC), that offer high decoding throughput at low implementation complexity and they are considered in many applications and communication standards.

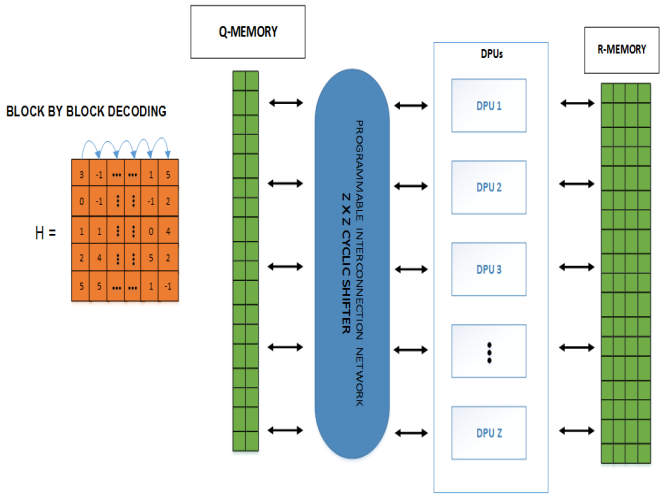
The ntLDPCD IP core implements an approximation of the log-domain LDPC iterative decoding algorithm. The core is highly reconfigurable and it is able to support different sub-matrix sizes (Z) of QC-LDPC-BC, that are tailored for specific applications. It also supports varying on the fly code rates, decoding iterations and input data width. The implementation is flexible, high speed with a simple interface for easy integration in SoC applications.

Applications

The ntLDPCD core can be used in a variety of applications, including:

- Digital Video Broadcasting: DVB-S2, DVB-S2X, DVB-T2, DVB-C2.
- Deep-space satellite missions (CCSDS).
- Next Generation Wired Home: Networking G.9960/G.9961 (G.hn).
- WiMax (IEEE 802.16e).
- WiFi (IEEE 802.11n - IEEE 802.11ac).
- WiGig (IEEE 802.11ad).
- WPAN (IEEE 802.15.3c).
- Hard disks.
- 10 Gigabit Ethernet - 10GBASE-T (IEEE 802.3an).
- CMMB (China Multimedia Mobile Broadcasting).

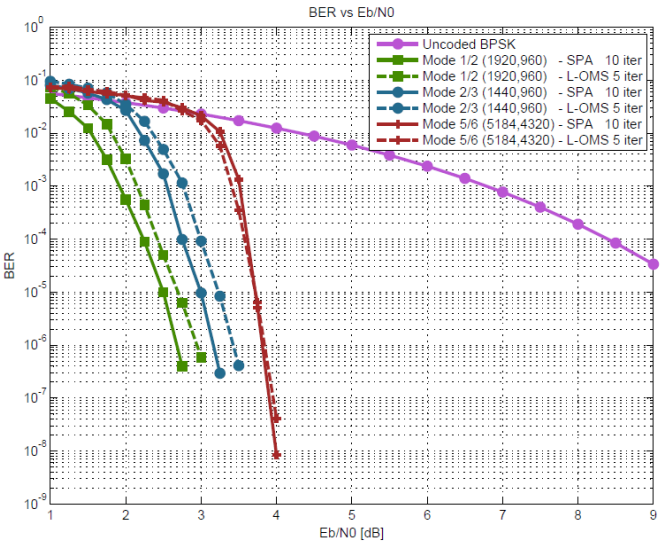
Architectural diagram



Features

- Fully configurable, high throughput, LDPC Decoder.
- Supports different LDPC coding standards.
- Variable on the fly input data width, code rates, decoding iterations.
- Supports variable sub-matrix sizes (Z).
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies.

Error correction performance



Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntLDPCD core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL source code or FPGA netlist.
- VHDL test benches and example configuration files.
- Matlab model.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntLDPCD core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request.

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