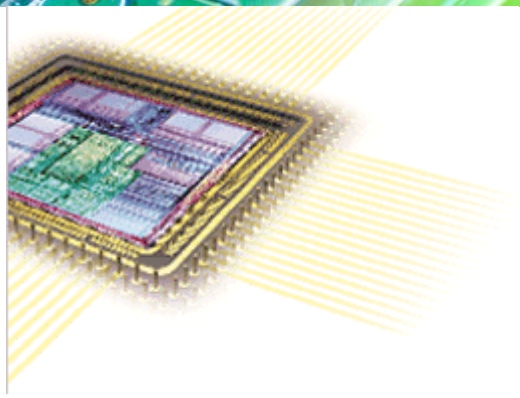
ntLDPCE

Fully Configurable LDPC Encoder



In channel coding redundancy is inserted in the transmitted information bit-stream. This redundant information is used in the decoder to eliminate the channel noise. The error correction capability of a FEC system strongly depends on the amount of redundancy as well as on the coding algorithm itself. The Low Density Parity Check (LDPC) codes are powerful, capacity-approaching channel codes and have exceptional error correction capabilities. The algorithm's high degree of parallelism enables efficient, high-throughput hardware architectures.

The ntLDPCE core implements the LDPC Block Codes (LDPC-BC). These LDPC codes are based on block-structured LDPC codes with circular block matrices. The entire parity check matrix can be partitioned into an array of block matrices, each block matrix is either a zero matrix or a right cyclic shift of an identity matrix. The parity check matrix designed in this way can be conveniently represented by a base (block) matrix. The main advantage is that they offer high throughput at low implementation complexity and they are used in many applications and communication standards.

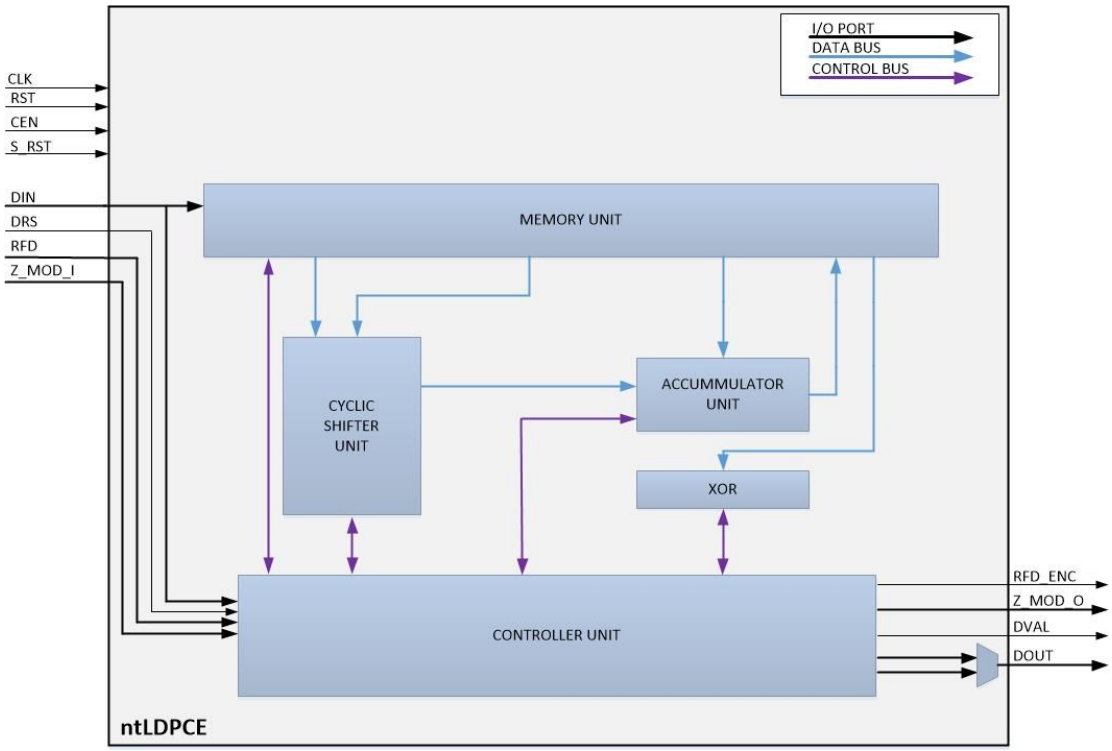
The ntLDPCE core is fully configurable and compliant with various wireless and wireline communication standards including ITU-T G.9960 (G.hn), IEEE 802.16e (WiMAX), IEEE 802.11n/ac (WiFi) etc. Particularly, the core is highly reconfigurable and it is able to support different sub-matrix sizes (Z) of LDPC-BC, that are tailored for specific applications. It also supports varying on the fly code rates. The implementation is flexible, high speed, area optimized and has a simple interface for easy integration in SoC applications.

Applications

The ntLDPCE core can be used in a variety of applications, including but not limited to:

- Next generation Wired Home: Networking G.9960/G.9961 (G.hn).
- Digital Video Broadcasting: DVB-S2, DVB-S2X, DVB-T2, DVB-C2.
- Deep-space satellite missions (CCSDS).
- WiMax (IEEE 802.16e).
- WiFi (IEEE 802.11n - IEEE 802.11ac).
- WiGig (IEEE 802.11ad).
- WPAN (IEEE 802.15.3c).
- Hard disks.
- 10 Gigabit Ethernet - 10GBASE-T (IEEE 802.3an).
- CMMB (China Multimedia Mobile Broadcasting).

Block Diagram



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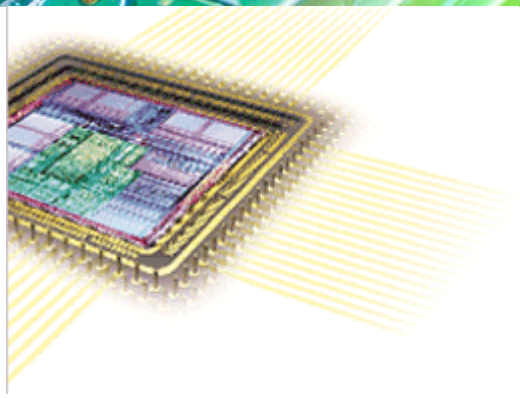
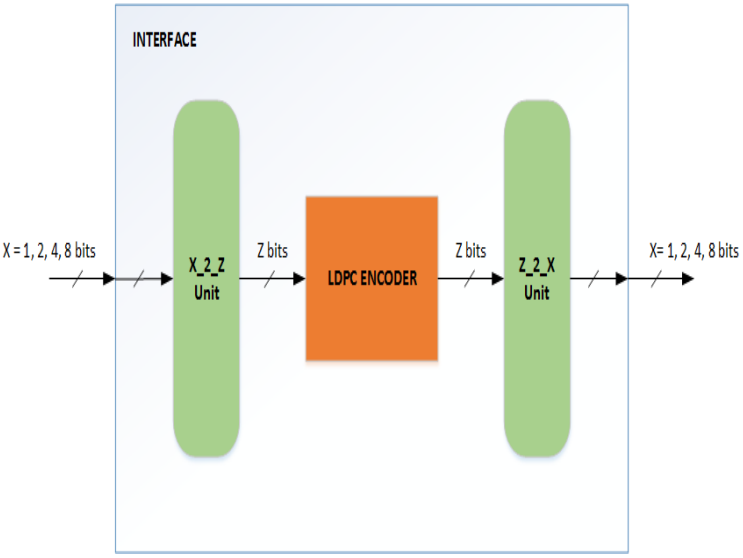


Interface Block

An optional interface block instantiates the LDPC encoder enabling a flexible exchange of data. The internal data parallelism of the LDPC encoder is Z bits. Particularly, for the ITU-T G.9960 standard, the range of sub-matrix size (Z) is 14 to 360 bits, depending on the mode of operation used. The interface can support X=1, 2, 4 or 8 information bits in parallel. The interface block is optimized to provide optimal performance with a small overhead in resources and throughput.



Features

- Fully configurable, high throughput, highly optimized silicon implementation.
- Supports different LDPC coding standards.
- Variable on the fly code rates.
- Supports variable sub-matrix sizes (Z).
- Flexible interface for easy system integration.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements. The implementation details and performance metrics of the ntLDPCE core configured for ITU-T 9960 G.hn standard are shown in the tables below.

Silicon Vendor	Device	Resources [1]	Fmax (MHz)
Xilinx	Kintex 7	4018 CLB Slices / 31 Block Rams	203

1) The resources include the interface of the ntLDPCE core.

Information Throughput

Mode	Code Rate	(code_len,info_len)	TP[2] (Gbps) Z bits parallel	TP[3] (Gbps) 8 bits parallel
1	(1/2)H	(336,168)	0,310	0,272
2	(1/2)S	(1920,960)	1,355	0,748
3	(1/2)L	(8640,4320)	1,458	0,745
4	(2/3)S	(1439,960)	1,397	0,998
5	(2/3)L	(6480,4320)	1,447	0,980
6	(5/6)S	(1152,960)	1,442	1,249
7	(5/6)L	(5184,4320)	1,479	1,243

2) The information throughput is for an LDPC encoder with parallelism of Z information bits without the optional interface block.

3) The information throughput is for an LDPC encoder including the optional interface block configured for X=8.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntLDPCE core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Matlab model.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntLDPCE core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com.
Noesis Technologies products are purchased under a License Agreement, copies of which are available on request.

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