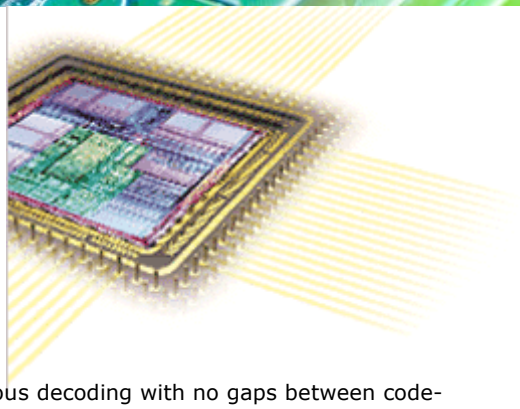
ntRSD

Configurable Reed Solomon Decoder



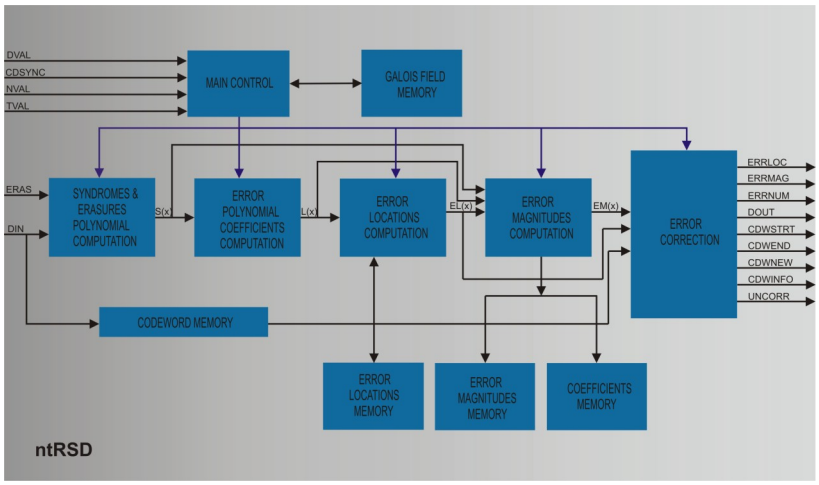
In channel coding redundancy is inserted in the transmitted information bit-stream This redundant information is used in the decoder to eliminate the channel noise. The error correction capability of a FEC system strongly depends on the amount of redundancy as well as on the coding algorithm itself. ntRSD core implements a time-domain Reed-Solomon decoding algorithm. The core is parameterized in terms of bits per symbol, maximum codeword length and maximum number of parity symbols. It also supports varying on the fly shortened codes. Therefore any desirable code-rate can be easily achieved rendering the decoder ideal for fully adaptive FEC applications. ntRSD core supports erasure decoding thus doubling its error correction capabillity. The core also supports continuous or burst decoding. The implementation is very low latency, high speed with a simple interface for easy integration in SoC applications.

Applications

The ntRSD core can be used in a variety of applications, including:

- Wireless broadband – IEEE 802.16.
- Gigabit Optical Networks (2.5, 10 & 40G) – ITU-T G.795.
- GPON (G.984).
- DVB (ETS 300 421 – Satelite).
- DVB (ETS 300-429 – Cable).
- ADSL (ANSI T1.413, ETS 101 388).
- DECT (ETS 300 175).
- Intelsat Earth Stations – IESS-308.
- Space Telemetry Systems.

Block Diagram



Features

- Fully configurable, time-domain, high throughput, Reed Solomon Decoder.
- Supports different Reed Solomon coding standards.
- Variable on the fly code rate adaptation by varying codeword length and/or number of parity symbols.
- Variable bits per symbol.
- Variable codeword length on a codeword by codeword basis.
- Variable number of errors corrected on a codeword by codeword basis.
- Supports shortened codes.
- User configured primitive polynomial.
- User configured generator polynomial.
- Supports error and erasure decoding.
- Single or multiple symbol rate clock.
- Continuous decoding with no gaps between codewords.
- Predictable decoder latency.
- Counts number of errors and flags uncorrectable codewords.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources [1]	Fmax (MHz)
Xilinx	Virtex 5	1490 CLB Slices / 3 Block RAMs	174
Xilinx	Spartan 3	2810 CLB Slices / 3 Block RAMs	50
Xilinx	VirtexII-Pro	2765 CLB Slices / 3 Block RAMs	88
Altera	Stratix-GX	5865 LCs / 3 Block RAMs	83
TSMC	0.18 um	25 K gates [2] / 12 K RAM bits	200

1) Implementation data are for a fully configurable decoder with T=8. 2) Equivalent NAND2 gate count.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntRSD core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- C++ model.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntRSD core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

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