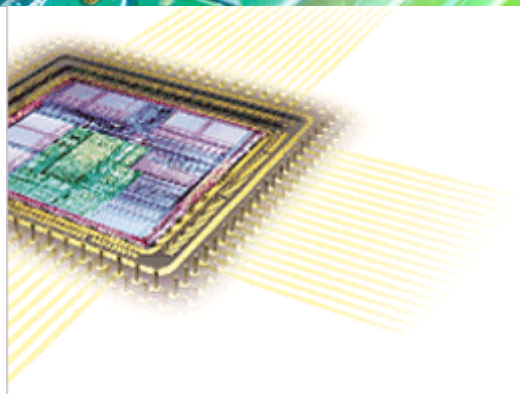
ntSOD

Configurable Soft Output Demapper

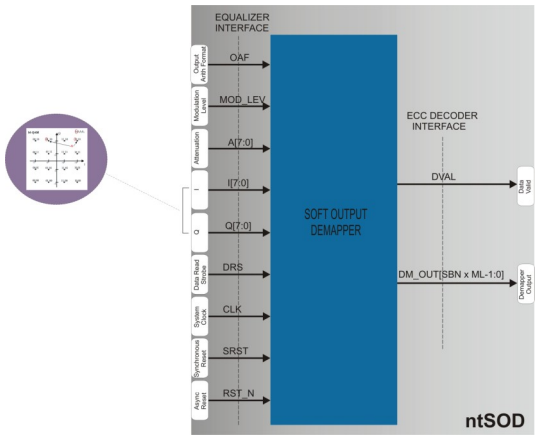


Noesis Technologies Soft Output Demapper is a structural element of any modern telecom system. The receiver extracts the phase and magnitude of the carrier signal. Subsequently a decision must be taken on the actual transmitted bits. Due to channel noisy conditions, the received signal has been distorted and there are positional errors on the constellation points. The ntSOD Soft Output Demapper IP Core implements the LLR (Log Likelihood Ratio) algorithm to convert the received distorted modulated signal from its complex I, Q form to a bit stream. It identifies the actual transmitted symbol bits and assigns to each bit a level of confidence in the format of a soft value. It supports various modulation levels such as BPSK, QPSK, 16 QAM and 64 QAM. This soft-bit information can be subsequently used during ECC decoding process by a soft-input ECC decoder such as Viterbi Decoder. Soft decision ECC decoding can provide a coding gain of 2 dB for 3 soft-bits per encoded bit or 2.2 dB for 4 soft bits per encoded bit when compared with hard decision ECC decoding. The soft-bit information can be configured in sign-magnitude or 2's complement format.

Applications

The ntSOD core can be used in any telecom application that requires an accurate and efficient log likelihood ratio method for calculating soft output information.

Block Diagram



Features

- Soft output demapper based on the LLR (Log Likelihood Ratio) algorithm.

FLEXIBILITY

- Parameterized number of soft bits per symbol .
- Parameterized architecture depending on supported modulation levels for optimum resources utilization.
- Programmable modulation level.
- Supports BPSK, QPSK, 16 QAM, 64 QAM constellations.
- Supports 2's complement of sign-magnitude soft output arithmetic format.

HIGH PERFORMANCE

- Compact design that requires approximately 500 Virtex-2 CLB slices.

OTHERS

- Fully synchronous design, using single clock.
- Silicon proven in Xilinx FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to Xilinx FPGA technology for various applications. Please contact us for implementation estimates for other technologies. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device [1]	Resources	Fmax (MHz)
Xilinx	Virtex-2	512 CLB Slices	50

1. Speed grade -5.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntSOD core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntSOD core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

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