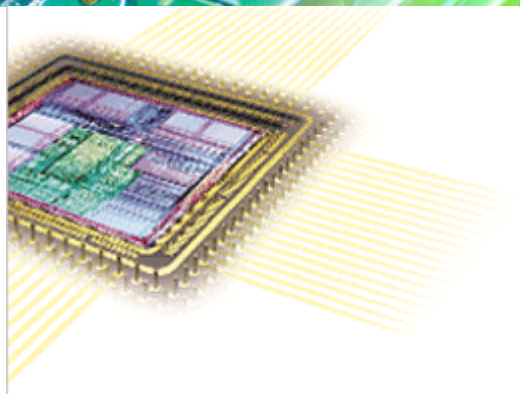
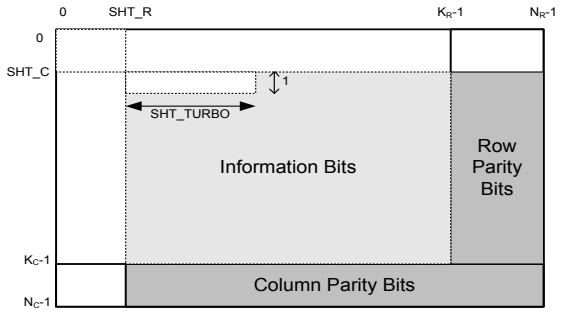
ntTPC

Configurable Turbo Product Codec



In channel coding redundancy is inserted in the transmitted information bit-stream. This redundant information is used in the decoder to eliminate the channel noise. The error correction capability of a FEC system strongly depends on the amount of redundancy as well as on the coding algorithm itself. TPCs perform well in the moderate to high SNRs because the effect of error floor is less. As TPCs have more advantage when a high rate code is used, they are suitable for commercial applications in wireless and satellite communications. The ntTPC Turbo Product Codec IP core is consisted of the Turbo Product Encoder (ntTPCe) and the Turbo Product Decoder (ntTPCd) blocks. The product code C is derived from two/three constituent codes, namely C1, C2 and optionally C3. The information data is encoded in two/three dimensions. Every row of C is a code of C2 and every column of C is a code of C1. When the third coding dimension is enabled, then there are C3 C1*C2 data planes. The ntTPC core supports both e-Hamming and Single Parity Codes as the constituent codes. The core also supports shortening of rows or columns of the product table, as well as turbo shortening. Shortening is a way of providing more powerful codes by removing information bits from the code. In figure below, we can see how a (NC-SHT_C, KC-SHT_C) × (NR-SHT_R, KR-SHT_R) code is derived from the original (NC, KC) × (NR, KR) code.



The ntTPCe core receives the information bits row by row from left to right and transmits the encoded bits in the same order. It consists of a row, column and 3D encoder. The row encoder encodes the data row-wise (C2). The encoded data produced from the row encoder are stored in an intermediate memory and reordered in a column-wise fashion. Once a full column has been written in the memory, the data are encoded column-wise by the column encoder (C1). When 3d encoding is employed, the encoded data produced from the column encoder are stored in an intermediate memory and reordered in a 3d-plane-wise fashion. The C3 data planes are encoded by an SPC(4,3) encoder (C3). Before output encoded information data are being reordered in row-wise fashion.

The ntTPCd decoder receives soft information from the channel in the 2's complement number system and the input samples are received row by row from left to right. The decoded soft information is output in the same order. The implemented decoding algorithm computes the extrinsic information for every dimension C1, C2, C3 by iteratively decoding words that are near the soft-input word. These words are called test patterns and their number is pre-configurable. All C1, C2, C3 words decoding takes place in a main decoding unit, the programmable elementary Soft Input Soft Output (SISO) decoder. An advanced scalable and parametric design approach produces custom design versions tailored to end customer applications design tradeoffs.

Applications

The ntTPC cores can be used in a variety of applications, including:

- Wireless broadband—IEEE 802.16 (Wimax)
- Optical transmission systems—FSO
- Satellite Communication Systems—VSAT modems
- Deep space communications—CCSDS

Features

- Encoder and decoder, support extended Hamming (256,247), (128,120), (64,57), (32,26), (16,11), (8,4) and Single Parity (256,255), (128,127), (64,63), (32,31), (16,15), (8,7) constituent error correcting codes.
- 3D encoding/decoding support with Single Parity (4,3) constituent code.
- Highly programmable and parameterizable cores in terms of error correction capability, code rate, decoding iterations, decoding test patterns and scalability of design architecture.
- Minimum system resources utilization and maximum resources reuse with one Single TPC elementary decoder instance for low power applications, producing up to 10Mbps information throughput (100Mhz – 4 decoding iterations).
- Small area footprint of the elementary decoder also allows an alternative high throughput design approach with a number of cascaded / parallelized elementary decoders (plus the extra memories overhead), in order to reduce internal data re-iterations.
- Flexible generic architecture with various combinations of parallelism options providing any desired application trade-off between area, performance and throughput rates.
- Decoding algorithm achieves competitive performance results with the minimum possible test patterns and decoding iterations.
- Bit serial encoder input/output interface.
- Soft input – soft output (SISO) serial decoder interface.
- Flexible and programmable code rates, ranging from 0.1875 to 0.9922 (without shortening).
- Additional programmability support for shortening of any selected code rate.
- Programmable number of algorithmic iterations.
- Simple yet robust encoder and decoder cores interface for optimum data flow control.
- Synchronous single clock design.
- Silicon proven in ASIC and Xilinx FPGA implementation technologies.

Implementation details

The ntTPCe and ntTPCd cores have been synthesized using Xilinx ISE Design Suite tools. The cores have been targeted to Kintex 7 XC7K410T-2 FFG900 device with a default balanced optimization strategy between area and timing. The area and performance metrics produced are summarized in the following graphs illustrating the various design trade-offs.

The implementation details for the configurable ntTPCe core range from:

- The compact 64 bits/word—Non3D encoder (1st line), to
- The larger 256 bits/word—3D encoder (2nd line).

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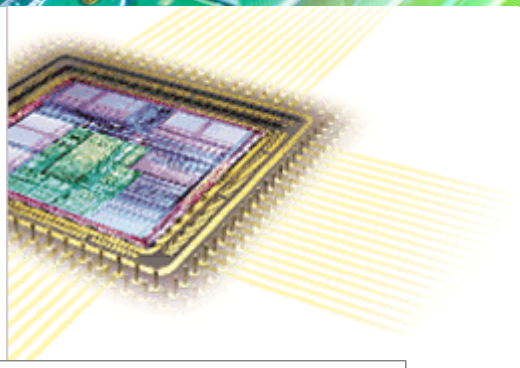
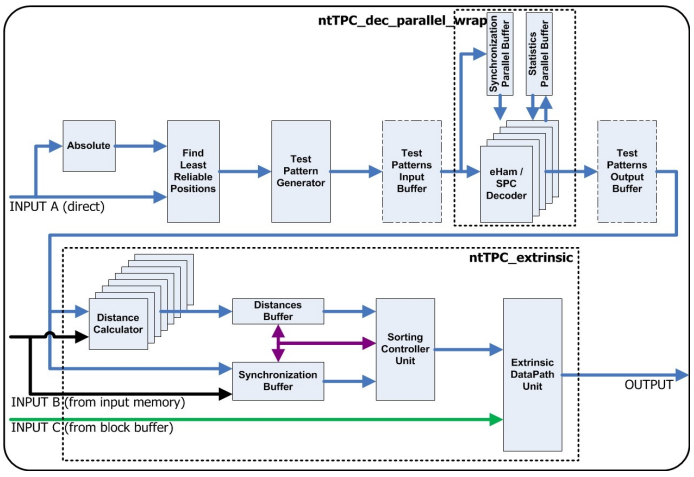
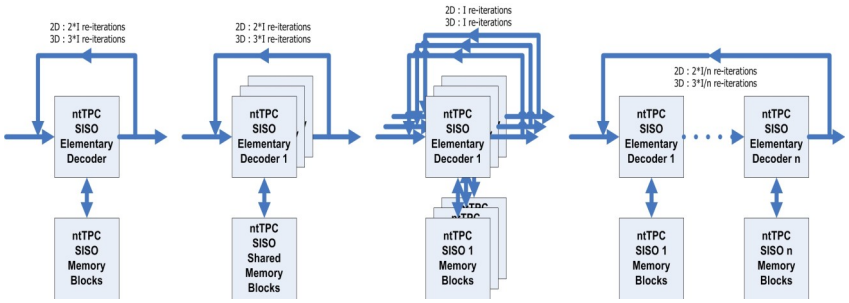


Silicon Vendor	Device	Resources	Fmax (MHz)
Xilinx	Kintex 7 XC7K410T-2	334 Slices / 9216 Memory Bits	224
Xilinx	Kintex 7 XC7K410T-2	439 CLB Slices / 215040 Memory Bits	208

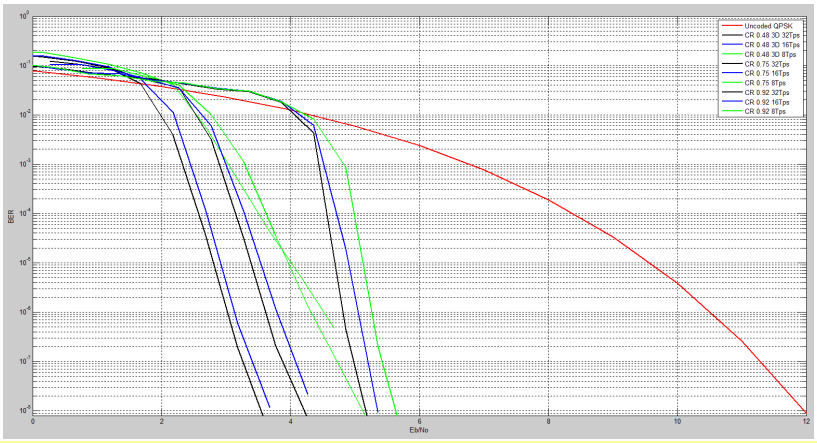
The architecture of one elementary SISO decoder shown below is parameterizable in terms of maximum constituent code size (64,128,256 bits), optional 3D codes support and maximum parallel test patterns processing (8,16,32) and soft bits.

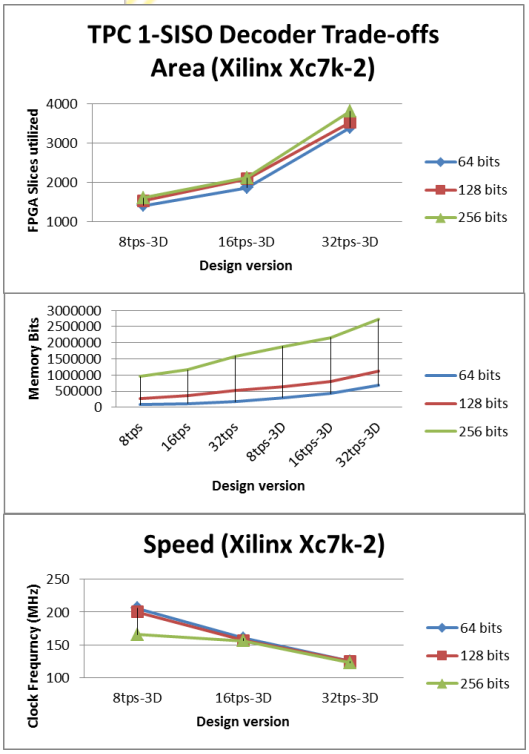


Depending on system trade-offs / requirements, one or more SISO decoders may be used in one of the following schemes:



For the various configurations of the single SISO decoder architecture, the following performance metrics and implementation details are produced, as shown in the following figures:





Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntTPC core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL source code or FPGA netlist.
- VHDL test bench and example configuration files.
- C++ model.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntTPC core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request.

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