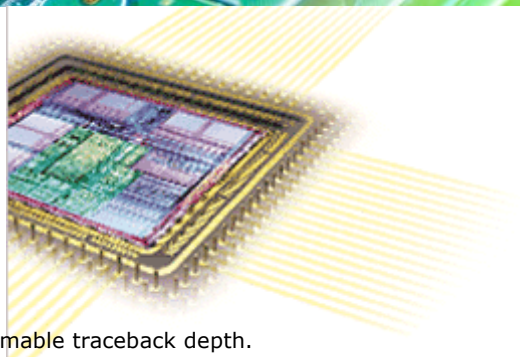
# ntVIT

## Configurable Viterbi FEC System



Convolutional FEC codes are very popular because of their powerful error correction capability and are especially suited for correcting random errors. The most effective decoding method for these codes is the soft decision Viterbi algorithm. ntVIT core is a high performance, fully configurable convolutional FEC core, comprised of a 1/N convolutional encoder, a variable code rate puncturer/depuncturer and a soft input Viterbi decoder. Depending on the application, the core can be configured for specific code parameters requirements. The highly configurable architecture makes it ideal for a wide range of applications. The convolutional encoder maps 1 input bit to N encoded bits, to generate a rate 1/N encoded bitstream. A puncturer can be optionally used to derive higher code rates from the 1/N mother code rate. On the encoder side, the puncturer deletes certain number of bits in the encoded data stream according to a user defined puncturing pattern which indicates the deleting bit positions. On the decoder side, the depuncturer inserts a-priori-known data at the positions and flags to the Viterbi decoder these bits positions as erasures. The Viterbi decoder uses a maximum-likelihood detection recursive process to correct errors in the data stream. The Viterbi input data stream can be composed of hard or soft bits. Soft decision achieves a 2 to 3dB increase in coding gain over hard-decision decoding. Data can be received continuously or with gaps.

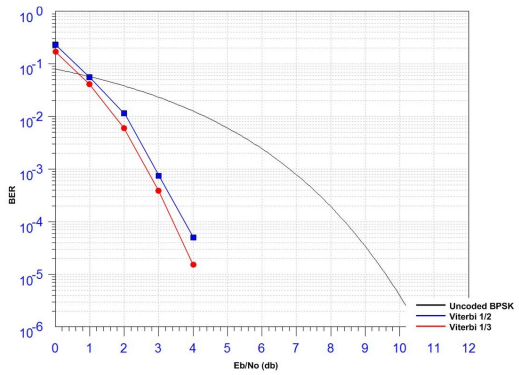
## Applications

The ntVIT core can be used in a variety of applications, including:

- 3G Wireless Base Stations.
- xDSL(ADSL,VDSL,HDSL,SDSL).
- WiMAX (IEEE 802.16e).
- Wireless LAN (IEEE 802.11).
- Wireless PAN (IEEE 802.15.3a).
- Cable Modems.

## Performance

The Viterbi decoder performance is typically illustrated with a BER vs SNR curve. The following figure demonstrates the BER vs SNR curve of a 1/2 and 1/3 rate Viterbi decoder, with constraint length equal to 7. As shown, a coding gain of 5 dB is achievable in rate 1/3 and 4.6 dB in rate 1/2 with a BER of $10^{-4}$ .




## Features

- Fully configurable, high throughput convolutional FEC system based on Viterbi Decoder algorithm.
- Supports different convolutional coding standards.
- Parameterizable constraint length, code rate, generator coefficients and soft bits.
- Parameterizable puncturing for full code rate control.
- Programmable traceback depth.
- Supports zero terminating and tail biting Viterbi decoding algorithm.
- Soft or hard decision decoding.
- Supports both continuous and burst input data flow.
- Supports both block and continuous based decoding.
- Fixed Viterbi decoder latency.
- Single or multiple symbol rate clock.
- Continuous decoding with no gaps between codewords.
- Predictable decoder latency.
- Area efficient design.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

## Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

| Silicon Vendor | Device | Resources [1] | Fmax (MHz) |
|---|---|---|---|
| Xilinx | Virtex 5 | 2200 CLB Slices / 4 BRAMs | 150 |
| Altera | Stratix-III | 7384 ALUTs / 8 M144K BRAMs | 100 |
| TSMC | 0.18 um | 50 K gates [2] / 9K RAM bits | 230 |

1) Implementation data are for a convolutional code of ½ rate and constraint length 7. 2) Equivalent NAND2 gate count.

## Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntVIT core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- C++ model.
- Comprehensive technical documentation.
- Technical support.

## Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

## Ordering information

To purchase or make any further inquiries about our ntVIT core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request.

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