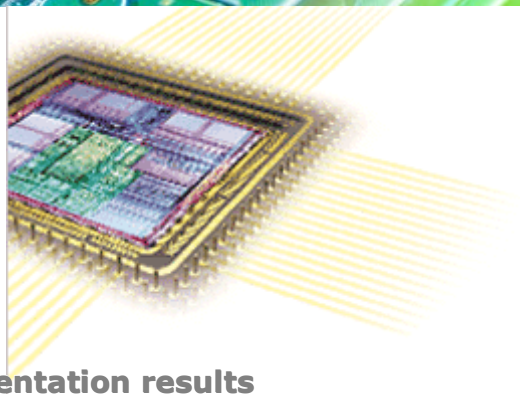
ntAWGN

Gaussian Channel Emulator



The performance evaluation of a telecom system under the presence of noise using software can be very time consuming. Whereas the noise generation in the analog domain is an easy task, in digital domain the generation of AWGN is a much more complex task. The ntAWGN core provides a hardware implementation of an accurate AWGN noise generator that can be used in the efficient performance evaluation of a digital communication system. The core generates AWGN with the following characteristics:

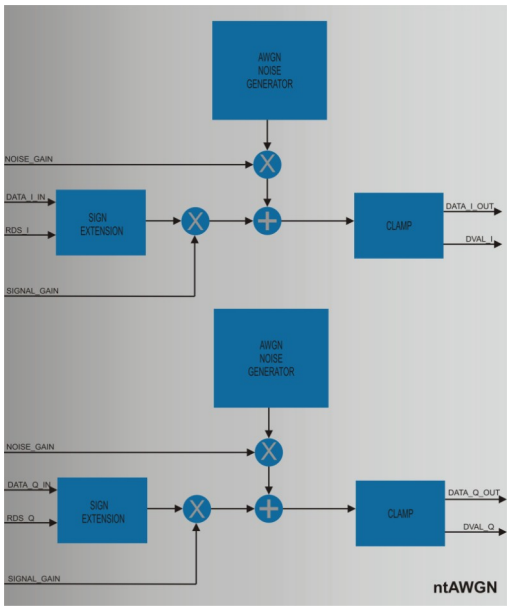
- Random distribution in the range of [-4σ...4σ], where σ is the standard deviation.
- Resolution 10 bits.
- Periodicity up to 2^{60} samples.
- Bit error insertion in the range of 0.5 to 10^{-10}.

Bit errors are generated by adding a white gaussian noise variable to the input bit stream. The number of bit errors and therefore the noise level is controlled by adjusting the standard deviation of the AWGN and/or the input signal amplitude. The ntAWGN core is comprised of two independent white gaussian noise generators that are used to add noise to a complex signal represented by two 10-bit I and Q samples.

Applications

- Any telecom application that requires accurate emulation of an AWGN channel.
- Bit-error rate measurement systems.

Block Diagram



Features

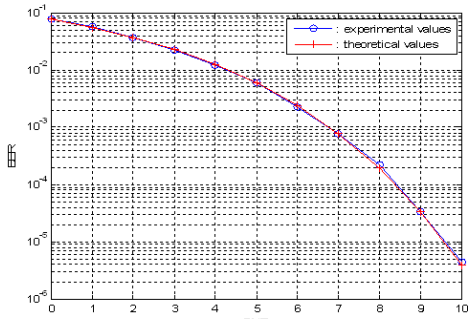
- Fully configurable, high throughput, Gaussian channel noise generator.
- Generates randomly distributed bit errors.
- High accuracy by combining Box-Muller algorithm and central limit methods.
- Provides a fast and low-cost channel emulator platform.
- Variable standard deviation.
- Programmable noise level.
- Normal distribution up to 4 times the standard deviation.
- Parameterized arithmetic precision.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources [1]	Fmax [1] (MHz)
Xilinx	Virtex-E	953 CLB Slices	126
TSMC	0.18 um	8500 gates [1]	300

1. Equivalent NAND2 gate count.



Theoretical vs ntAWGN BER vs SNR for uncoded BPSK

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntAWGN core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Matlab model.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntAWGN core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request.

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