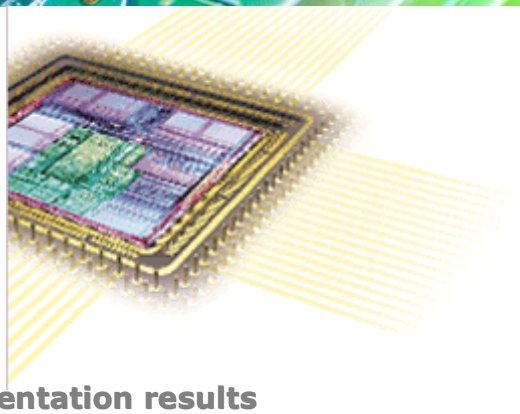
ntHDLC

Single Channel HDLC Controller



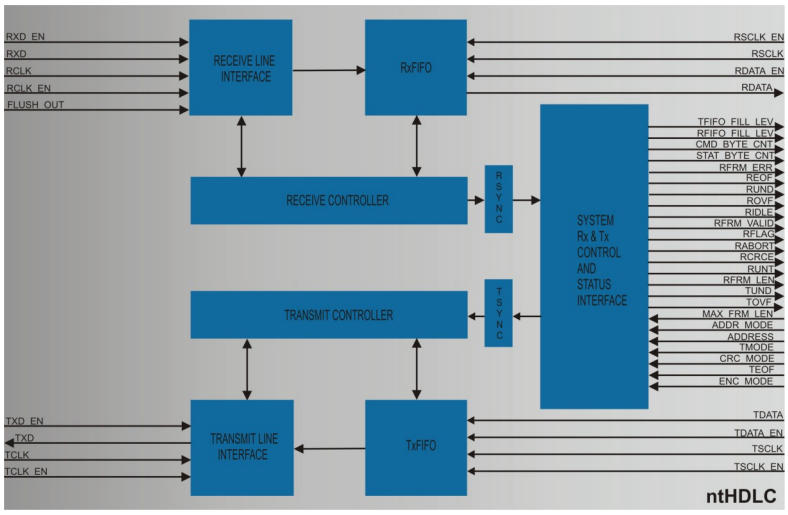
Noesis Technologies ntHDLC single channel High-Level Data Link Controller (HDLC) is a full-duplex transceiver with independent transmit and receive units for synchronous framing bit-level HDLC protocol operations. The ntHDLC can handle interframe and delimiting flags, frame check sequence based on CCITT CRC16/CRC32 polynomial, normal or transparent transmission modes, abort generation and detection. The system interface is very flexible and can be adapted towards FIFO, uP, or DMA controllers. The transmit and receive units and their associated control and status logic are independent. This partitioning strategy enables the Tx and Rx units to be instantiated in different place and/or level of the design hierarchy. Each unit (Tx, Rx and back-end interface) has its own clock domain with synchronous clock enable. Communication between the various clock domains is achieved via synchronization logic blocks.

Applications

The ntHDLC core can be used in a variety of applications, including:

- Embedded applications in Telecom systems.
- X.25 (LAPB), Q.921(LAPD) applications.
- Point to point communication links.
- ISDN, Q.922 Frame Relay, PBX, WAN.

Block Diagram



Features

- Single port synchronous serial line interface.
- Flag/Abort Generation/Detection.
- Zero Insertion/Deletion.
- Non-octet alignment detection.
- CCITT CRC-16 Generation and Checking.
- NRZ/NRZI encoding/decoding.
- Transparent mode support.
- Receive FIFO overrun detection.
- Transmit FIFO underrun detection.
- Frame status and frame length indicators.
- Runt frame detection.
- Seperate clocks for Tx and RX interfaces.
- Supports fllag in interframe-time fill.
- 8-bit parallel back-end interface.
- Fully synchronous design.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources [1]	Fmax (MHz)
Xilinx	Spartan 3	460 CLB Slices / 10 Block RAMs	80 (tclk) 126 (rclk) 140 (tsclk) 140 (rsclk)
Xilinx	Virtex 5	200 CLB Slices / 10 Block RAMs	130 (tclk) 230 (rclk) 310 (tsclk) 313 (rsclk)
Altera	Stratix-III	600 ALUTs / 10 M9K RAM blocks	72 (tclk) 139 (rclk) 184 (tsclk) 133 (rsclk)
TSMC	0.18 um	5800 gates [2] / 74 K RAM bits	340 (tclk) 400 (rclk) 330 (tsclk) 340 (rsclk)

1. The implementation uses 2 FIFOs of 4096 words x 9 bits/word size each. Please contact us to provide results for different FIFO size implementations.
2. Equivalent NAND2 gate count.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntHDLC core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntHDLC core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

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