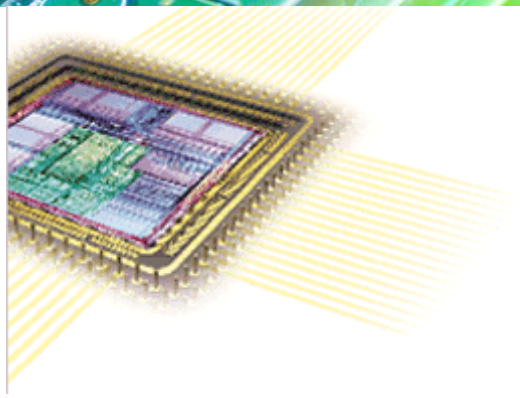
ntINT_DEINT

Configurable Interleaver/Deinterleaver



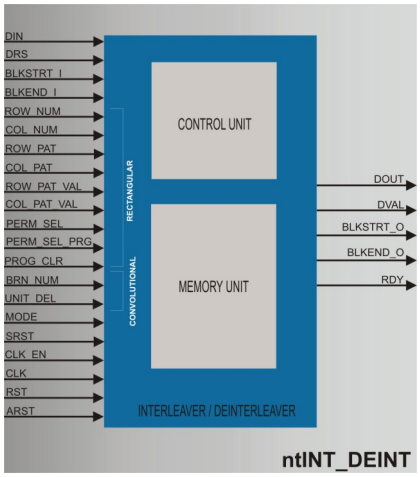
Error detection and correction are perhaps the most important quality factors to observe when evaluating a digital transmission system. A system's noise environment can cause errors in the transmitted message degrading the credibility of the system. Digital communications systems designers can choose among many types of error-correction codes to reduce the effect of errors in stored or transmitted data. Most common error correcting codes are designed to correct *random errors* i.e. errors that are independent of each other and distributed uniformly in time. However errors that occur in *bursts* ,i.e. errors that occur sequentially in time and as groups, tend to be problematic for most FEC schemes. Block codes, and in particular Reed-Solomon codes, can handle burst errors effectively only as long as the number of errors per data block is below a certain limit. Interleaving is a simple, yet powerful technique that can be used to extend the error correcting capability of a Reed-Solomon code and other FEC codes. The ntINT_DEINT interleaver/de-interleaver subsystem rearranges the encoded symbols over multiple data blocks. This effectively spreads out long burst noise sequences so they appear to the decoder as independent random symbol errors or shorter more manageable burst errors. This is achieved by using the interleaving function that changes the order of data before the transmission on the channel so that any adjacent symbols are well separated during transmission. The symbols are then reordered by the deinterleaving function during reception. Block and Convolutional are the most frequently used interleaver types.

Applications

The ntINT_DEINT core can be used in a variety of applications, including:

- Wireless broadband – IEEE 802.16.
- DVB (ETS 300 421 – Satelite).
- DVB (ETS 300-429 – Cable).
- ATSC

Block Diagram



Features

- Fully configurable, convolutional and rectangular interleaver/ deinterleaver.
- Compliant to a variety of industry standards.
- Rectangular Block (de) interleaver function fully parameterized :
  - Block size
  - Number of rows
  - Number of columns
  - Rows and/or columns permutations
- Convolutional (de) interleaver function fully parameterized :
  - Number of branches
  - Configurable branch length
- Variable block length on a block by block basis.
- Configurable number of bits per symbol.
- Handshaking logic for I/O data flow control.
- Fully synchronous design, using single clock.
- Silicon proven in ASIC and FPGA technologies for a variety of applications.

Implementation results

The core has been targeted to both ASIC and FPGA technologies for various applications. Noesis Technologies can also deliver netlist versions of the core optimized to specific area resources and performance requirements.

Silicon Vendor	Device	Resources [1]	Fmax (MHz)
Altera	StratixIII	161 ALUTs / 3 M144K BRAMs	152
TSMC	0.18 um	1500 gates [2] / 140 K RAM bits	360

1) Implementation data are for a block (de)interleaver core with 64 rows, 64 columns, 16 bits per symbol and 10 permutation patterns. 2) Equivalent NAND2 gate count.

Deliverables

Noesis has engaged an "open" licensing philosophy in order to allow maximum technology transfer to our client's engineering teams and to facilitate the integration of our IP cores into our client's product. Various licensing models are available. The ntINT_DEINT core is available as a soft core (synthesizable HDL) or as a firm core (netlist for FPGA technologies). The following deliverables are included:

- Fully commented synthesizable VHDL or Verilog source code or FPGA netlist.
- VHDL or Verilog test benches and example configuration files.
- Comprehensive technical documentation.
- Technical support.

Support

Technical support by phone or email is included. First year of maintenance is also included. Additional support and annual maintenance options are available.

Ordering information

To purchase or make any further inquiries about our ntINT_DEINT core, or any other Noesis Technologies products or services, contact us at info@noesis-tech.com. Noesis Technologies products are purchased under a License Agreement, copies of which are available on request .

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