NOESIS TECHNOLOGIES

*"Engineering is our choice in life, we are best to few things we do really-really well, to help makers of great products"*

**Overview :**

After many years of expert research and system design, **Noesis Technologies** brings you the power of the **C-Cubed ($C^3$) product-line**, based on formal, cutting-edge techniques. The $C^3$ synthesis framework enables hardware and system engineers to realize unprecedented productivity gains in designing & developing complex, portable, embedded and special-purpose computing systems, without strangling with the details of the target hardware.

**Our Vision :**

To offer state-of-the-art automated ESL E-CAD engineering methods and rapid design (IP) services to customers that reduce the design & development time **orders of magnitude** for the most complex and demanding computing applications ever.

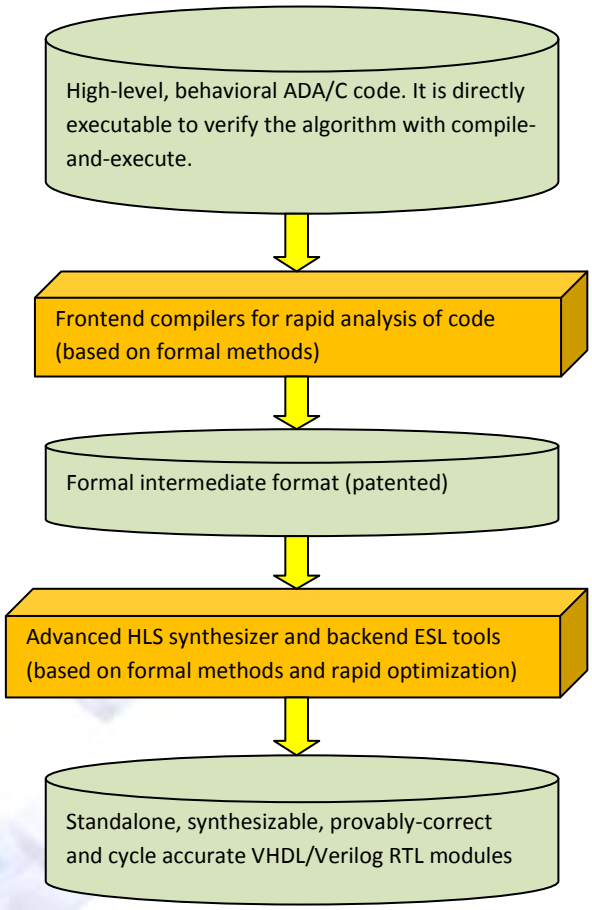
**Our Philosophy :**

Always be customer-oriented and work diligently to provide rapid design services, drawing form our experience, skills and advanced ESL methodology.

**The C-Cubed behavioral synthesizer**

The C-Cubed synthesizer is based on formal methods and includes the frontend (compiler) and the backend (HLS system). Currently there are ANSI-C and ADA frontends. More frontends (i.e UML) are expected in the immediate future. The backend synthesizer produces automatically cycle-accurate and fully synthesizable RTL VHDL or Verilog, depending on the choice of the user. More backend languages are expected in the immediate future such as System-C and cycle accurate C.

The whole C-Cubed product chain is based on formal methods, so the generated implementations are first-time-right and provably-correct in regard to the functionality of the input code. The design flow is shown in the following figure:




Our customers don't need to spend months or years in repetitive RTL and netlist verification cycles. With the formal nature of the C-Cubed synthesizer, only rapid compile-and-execute-based verification of the high-level behavioral program code is needed to correct functional bugs.

The backend synthesizer is driven by interface parameters, and resource constraints, so that

mapping on any rich (ASIC) or economic (FPGA) technology becomes reality in matter of hours.

**Our Offerings :**

- $C^3$ high-level ESL design methodology and **E-CAD tools**
- Rapid **design** & **prototyping** services
- Silicon-proof **IP blocks**, which are synthesizable and re-targetable to different technologies
- Software & hardware IP, in ADA, C, C++, Java, OpenCL, VHDL, Verilog

**with :**

- State-of-the-art high-level synthesis optimization and parallelism extraction
- Correct-by-construction implementations via formal compilation and optimization
- Support for mixed hardware + software system co-design and rapid development
- Extremely fast behavioral specification, modeling and verification, via executable specification models (high-level, algorithmic program code)
- What you code is what you get – based design flow and engineering philosophy
- Support for any ASIC and FPGA technologies

**Tool Features :**

The **$C^3$ toolset** features the following characteristics:

- Automatic generation of vendor-independent, and platform-free, synthesizable RTL VHDL/ Verilog
- Support of native algorithmic ADA code. Provably-correct generation of optimized (massively-parallel) hardware
- Use of technologically-mature and advanced compilation and formal HLS optimizations
- Tested on complex designs, such as MPEG video compression, cryptography, computer graphics, image/video processing, DSP
- Rapid ESL and system-level prototyping with support for all types of flat or hierarchical designs
- Simple/secure communication with handshake
- Hardware/software co-design and co-verification

**Methodology Advantages :**

The **$C^3$ toolset** offers customers the following advantages:

- Orders of magnitude faster modeling and verification of systems in comparison with RTL coding and debugging
- Support of as much as complex data-flow and control-dominated designs
- Automatic and formal generation of provably-correct synthesizable VHDL/Verilog HDL models
- Automatic, provably-correct generation of memory and any other external communication/ interface protocols in an automatic manner
- Rapid production of partitioning trade-offs, early in the spec & design cycle
- Interoperability with all standard simulators and RTL synthesizers for any ASIC or FPGA technology

**Licensing and availability**

Very flexible and cost effective licensing is available to our customers at very competitive levels, in regards with the existing ESL market. The following options are available:

- Free-of-charge availability for trials and academic users, via tool web-site.
- Commercial use as is via the tool web-site (per annum charge).
- Commercial use with full support via the tool web-site (per annum charge).
- Commercial use with local installation and support (per annum charge).
- Commercial use with local installation, support and all available annual updates (per annum charge).
- Perpetual license with local installation, support and all available updates (per annum charge).

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