Senior RTL Design Engineer – Telecom

At Noesis Technologies, we develop exciting state-of-the-art telecom technologies in the fields of IoT, Power Line Communication, Smart Grid / Smart Home, 5G Cellular, Data Security & Integrity, Wireless Sensor Networks as well as Wireless & Wireline transmission systems. We focus on the innovative design of hardware accelerated, reconfigurable, physical layer (PHY) baseband processors and in this framework of activity we are looking for a visionary, proactive and talented RTL Design Engineer to join our dynamic team. As a logic design engineer, you will be involved in all aspects of the design, from feasibility study, architectural definition, RTL design and verification up to silicon (FPGA or ASIC) bring-up and performance characterization.

Key Qualifications:

The ideal candidate will have five or more years of experience in logic design with the following skills required:

- RTL design using, VHDL, Verilog or System Verilog, assertion writing.
- Design of state machines, data paths, clock domain crossing logic, parameterized architectures.
- FPGA/ASIC Logic synthesis, timing constraints, static timing analysis.
- Design For Testability (DFT), understanding of scan concept and writing DFT friendly RTL.
- RTL/Gate level verification, writing self-checking, automated test benches.
- Experience in Matlab / Simulink modelling of telecom algorithms is a plus.

Education:

Bachelors or Masters Degree in Electrical Engineering or Computer Science.

Noesis Technologies offers competitive salary, excellent working environment, opportunity to design state-of-the-art technology and participate in large exhibitions around the world. The candidate will join our team in our RnD center, in Patras Science Park, Patras, Greece.

If you believe that you want to join our company, please forward your CV to info@noesis-tech.com

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